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2815

DOCKET NO. BAILLIE 2-2 PATENT

#26 IDS 11-12-03 restriction

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Matthew B. Baillie, et al.

Serial No.: 09/138,146

Filed: August 21, 1998

For: INTEGRATED CIRCUIT CARRIER AND METHOD OF MANUFACTURING AND INTEGRATED CIRCUIT

Group No.: 2815

Examiner: Sheila V. Clark

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, Alexandria, VA 22313, on 5-13-2003 (Date)
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Elizabeth Schumacher
(Signature of the person signing the certificate)
5-13-2003
(Date of Signature)

Sir:

INFORMATION DISCLOSURE STATEMENT

In accordance with 37 C.F.R. §1.56 and the provisions of 37 C.F.R. §§1.97 and 1.98 and §609 of the Manual of Patent Examining Procedure, Applicant hereby makes a disclosure of the patents, publications and other information listed below and on the accompanying form PTO-1449, which may be potentially material to the patentability of the invention disclosed in the above-referenced application. Pursuant to § 1.97(e) the Applicant hereby states that each item of information contained in the information disclosure statement was cited in a communication from

a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement.

Foreign Patent No.	Country	Date
05338616 A	JP	December 21, 1993
195 27 021 A1	DE	January 30, 1997
7 18499	JP	March 31, 1995

Applicant hereby certifies that each item of information contained in the Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the statement.

As attorney for the Applicant, I am signing below on the basis of the information supplied by an individual designated in § 1.56(c).

Respectfully submitted,

HITT GAINES & BOISBRUN, P.C.

Greg H. Parker
Registration No. 44,995

Date: 5-13-03

Hitt Gaines & Boisbrun, P.C.
P.O. Box 832570
Richardson, Texas 75083
(972) 480-8800

PTO/SB/08a (05-03)
Approved for use through 04/30/2003. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	09/138,146
Filing Date	August 21, 1998
First Named Inventor	Matthew B. Baillie, et al.
Art Unit	2815
Examiner Name	Sheila V. Clark
Attorney Docket Number	BAILLIE 2-2

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US-			
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FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3]-Number[4]-Kind Code[5] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
		JP 05338616 A	12/21/1993	Sharp Corp.		
		DE 195 27 021 A1	01/30/1997	Siemens		
		JP 7 18499	03 31 1995	--		

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional). 2 See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. 3 Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). 4 For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. 5 Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. 6 Applicant is to place a check mark here if English language Translation is attached.

EXAMINER'S OFFICE LETTER

FEB 28 2003
(Mailing Date: MAR 5 2003)

To: Applicant (Lucent Technologies Inc.)

Examiner : M. OOMACHI

"An Integrated Circuit Carrier And Method Of Manufacturing And Integrated Circuit"

Patent Application No. 221875/1999

The above-identified application is to be refused for the reason as put down. A reply to the present Office Action must be filed before JUN 5 2003 (three month extensible).

=Note=

1. The present inventions as set forth in claims 1-3, 5-7, 14 and 16-19 fall under Article 29, Paragraph 1, Item 3 of the Japanese Patent Law, because they are recognized to be the inventions as described in the listed References 1 published prior to this application.

2. The present inventions as set forth in claims 4, 8-13, 15 and 20 are unpatentable under Article 29, Paragraph 2 of the Japanese Patent Law, because of obviousness from the listed References 1-3.

3. This application does not satisfy the requirements as provided in Article 36, Paragraph 6, Item 2 of the Japanese Patent Law, because the specification is recognized to be defective on the undermentioned points.

=List of References=
Reference 1: German Patent Publication No. DE 195 27 021 A1
Reference 2: JP Laid-Open Patent Gazette No. 5-338616
Reference 3: JP Laid-Open Utility Model Gazette No. 7-18499
(Application No. 5-53604)

Note 1: Anticipation rejection
Listed reference 1

(1) With regard to claims 1-3 and 5-7 :
The listed reference 1 describes a belt 1 in which electric components are disposed on the bottom 5 of the depression 2. In the belt 1, the side wall 6 is descended from the depression bottom to the turning point located from the bottom downward and ascended to the edge of the depression, and then descended again to the turning point and the edge of the depression, thereby forming a shock-absorbing spring element 30. A shock-absorbing side wall is formed about the periphery of the depression 2.
Therefore, the features defined in claims 1-3 and 5-7 of the present application are not different from the above invention of the listed reference 1.
(2) With regard to claims 14 and 16-19 :
Listed reference 1

This reference discloses the invention as described above.
Therefore, the features defined in claims 14 and 16-19 are not different from those of the invention of this reference.

Note 2: Obviousness rejection

(1) With regard to claim 4:
Listed reference 1

In the listed reference 1, the side wall 6 is formed as a shock-absorbing spring element. Therefore, in the invention of this reference, locating the turning point of the outer side wall 6 more deeply than the turning point of the inner side wall 6 is an obvious design choice.

(2) With regard to claims 8-13 :
Listed reference 1

The Examiner understands that claim 8 defines a process of packaging an integrated circuit rather than a process of manufacturing an integrated circuit.
Claim 11 is withdrawn from consideration, since the expression "shipping the chip carrier" in this claim is indefinite as indicated in the following Note 3, Item (2) regarding the informality objections.
The expression "receiving a chip carrier" in claim 12 is indefinite as indicated in the following Note 3, Item (3) regarding the informality objections. Therefore, in this obvious rejection, this expression is interpreted as the meanings of "providing a chip carrier.

In the listed reference 1, it is recognized that the invention described in the above Note 1 is disclosed.
In a packaging of an integrated circuit using a carrier tape, providing a carrier tape, receiving an integrated circuit into a chip carrier and sealing an integrated circuit in a chip carrier are well-known technique. (If necessary, see "tape delivery portion 14", "loading operation portion 13" and "sealing portion 16" in the listed reference 2.)
Further, when an integrated circuit received in a carrier tape is mounted on a substrate, providing a carrier tape, retrieving an integrated circuit from the carrier tape and mounting the retrieved integrated circuit on a substrate are well-known technique. (If necessary, see "a reel 6 for providing a chip" and "an arm 9a for mounting a chip" in the listed reference 3.

The listed reference 1 discloses a belt 1 in which electric components are disposed on the bottom of the depression 2. Employing such a belt in the above steps well-known may easily be made by a person skilled in the art.

Therefore, the present inventions defined in claim 8-13 may easily be made by a person skilled in the art by combining the invention in the listed reference 1 with the above well-known technique.

(3) With regard to claim 15:
Listed reference 1

Locating the turning point of the outer side wall more deeply than the turning point of the inner side wall may easily be made by a person skilled in the art.

(4) With regard to claim 20:
Listed reference 1

The present invention defined in claim 20 may easily be made by a person skilled in the art on the basis of the invention of the listed reference 1 and the technique described in the above Note 1, Item (2).

Note 3: Informality objection

(1) With regard to claim 8:
This claim defines "A process of manufacturing an integrated circuit". However, the integrated circuit which has been completed is provided and positioned at the steps in this claim, and this claim defines the steps which is not included in a process of manufacturing an integrated circuit. It seems that this claim defines --a process of packaging an integrated

circuit--.

(2) With regard to claim 11:
This claim defines the step "shipping the chip carrier".
However, it is indefinite whether or not the chip carrier to be shipped has an integrated circuit.
In view of the specification, it seems that in such the chip carrier, an integrated circuit is received.
However, if the chip carrier with an integrated circuit is defined in this claim, the step in this claim is not included in a process of manufacturing an integrated circuit or a process of packaging an integrated circuit.

(3) With regard to claim 12:
This claim defines "receiving a chip carrier -".
However, this feature is indefinite.
The Examiner suggests correcting "receiving a chip carrier" to --providing a chip carrier--.

(4) With regard to claim 16:
This claim defines "the third position".
However, There is no antecedent basis of "the third position" in claim.

(5) With regard to claim 20:
This claim defines the step "moving the device from a first location to a second location in the carrier".
However, the features regarding this step is indefinite.

=Record of Search of the Prior Arts=
Technical Field of Search:
IPC Version 7
B65D 73/00-73/02
H05K 13/00-13/04
B65B 15/00-15/04

This record of search of the prior art does not constitute Reason for Refusal.